1. 5,802,554, Sep. 1, 1998, Method and system for reducing memory access latency by providing fine grain direct access to flash memory concurrent with a block transfer therefrom, Caceres, Ramon, New York, New York Bershad, Brian, Seattle, Washington Marsh, Brian D., New York, New York Douglis, Frederick, Somerset, New Jersey, Panasonic Technologies Inc., Princeton, New Jersey (02)

   CORE TERMS: memory, flash, processor, storage, stored, virtual, map, stable, bus, transferred...

2. 5,440,710, Aug. 8, 1995, Emulation of segment bounds checking using paging with sub-page validity, Richter, David E., San Jose, California Cohen, Earl T., Fremont, California Blomgren, James S., San Jose, California, Exponential Technology, Inc., San Jose, California (02), Date Transaction Recorded: Apr. 08, 1997 SECURITY INTEREST (SEE DOCUMENT FOR DETAILS). SILICON VALLEY BANK LOAN DOC. GROUP, NC816 3003 TASMAN DRIVE SANTA CLARA, CALIFORNIA 95054 Reel & Frame Number: 8447/0569Date Transaction Recorded: May 08, 1997 ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS). SILICON VALLEY BANK 3003 TASMAN DRIVE SANTA CLARA, CALIFORNIA 95054 Reel & Frame Number: 8495/0470Date Transaction Recorded: Oct. 06, 1997 FREE FORM TEXT SECURITY AGREEMENT SILICON VALLEY BANK 3003 TASMAN DRIVE SANTA CLARA, CALIFORNIA 95054 Reel & Frame Number: 8732/0564Date Transaction Recorded: Oct. 27, 1997 FREE FORM TEXT REASSIGNMENT + RELEASE OF SECURITY INTEREST IN PATENTS EXPONENTIAL TECHNOLOGY 2075 - ZANKER ROAD SAN JOSE, CALIFORNIA 95131 Reel & Frame Number: 8761/0916Date Transaction Recorded: Feb. 17, 1998 ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS). S3 INCORPORATED, INC. 2801 MISSION COLLEGE BLVD. SANTA CLARA, CALIFORNIA 95052-805 Reel & Frame Number: 8975/0935Date Transaction Recorded: May 14, 1998 FREE FORM TEXT CORRECTIVE ASSIGNMENT TO CORRECT ASSIGNOR & ASSIGNEE, PREVIO USLY RECORDED AT REEL 8975, FRAME 0935. S3 INCORPORATED P.O. BOX 58058 2801 MISSION COLLEGE BOULEVARD SANTA CLARA, CALIFORNIA 95052-805 Reel & Frame Number: 9114/0695

   CORE TERMS: segment, offset, virtual, sub-page, bit, memory, buffer, paging, byte, software...

3. 4,625,308, Nov. 25, 1986, All digital [IDMA] TDMA dynamic channel allocated satellite communications system and method, Kim, Kap S., Gaithersburg, Maryland Tisdale, William R. H., Baltimore, Maryland Andrews, Bruce S., Rockville, Maryland Nash, T. Randolph, Rockville, Maryland Kolodgie, Kathleen J., Rockville, Maryland Eiserike, Steven S., Rockville, Maryland, American Satellite Company, Rockville, Maryland (02), Date Transaction Recorded: Feb. 27,

1987 ASSIGNMENT OF ASSIGNORS INTEREST. AMERICAN SATELLITE COMPANY, 1801 RESEARCH BOULEVARD, ROCKVILLE, MD., 20850-3186, A CORP OF DE. Reel & Frame Number: 4671/0278Date Transaction Recorded: Jun. 21, 1993 MERGER (SEE DOCUMENT FOR DETAILS). GTE SPACENET CORPORATION 1700 OLD MEADOW ROAD MCLEAN, VA 22102 Reel & Frame Number: 6576/0315Date Transaction Recorded: Jun. 21, 1993 CHANGE OF NAME (SEE DOCUMENT FOR DETAILS). GTE SPACENET CORPORATION LEGAL DEPARTMENT 1700 OLD MEADOW ROAD MCLEAN, VIRGINIA 22102 Reel & Frame Number: 6581/0103Date Transaction Recorded: Jun. 21, 1993 CHANGE OF NAME (SEE DOCUMENT FOR DETAILS). GTE SPACENET CORPORATION LEGAL DEPARTMENT 1700 OLD MEADOW ROAD MCLEAN, VIRGINIA 22102 Reel & Frame Number: 6615/0615Date Transaction Recorded: Jun. 21, 1993 MERGER (SEE DOCUMENT FOR DETAILS). GTE SPACENET CORPORATION LEGAL DEPARTMENT 1700 OLD MEADOW ROAD MCLEAN, VIRGINIA 22102 Reel & Frame Number: 6615/0618

CORE TERMS: serial, map, bit, input, bus, buffer, switch, subsystem, burst, message...

Source: Utility Patents
Search Terms: read only w/3 executable and memory w/2 map!
View: CITE
Date/Time: Monday, March 29, 1999 - 9:43 AM EST

*Pat. No. 5802554, **

5,802,554

GET 1st DRAWING SHEET OF 4

Sep. 1, 1998

Method and system for reducing memory access latency by providing fine grain direct access to flash memory concurrent with a block transfer therefrom

INVENTOR: Caceres, Ramon, New York, New York
Bershad, Brian, Seattle, Washington
Marsh, Brian D., New York, New York
Douglis, Frederick, Somerset, New Jersey

CORE TERMS: memory, flash, processor, storage, stored, virtual, map, stable, bus, transferred...

ABST:

... access to the flash memory. In addition, concurrently with satisfying the data request directly from the flash memory, a block transfer is initiated from the flash memory to the main memory. Once the block transfer is completed, a **memory map,** such as an address translation table, is updated to indicate that the data now resides in the more convenient source of data-the main memory. Accordingly, subsequent data requests, for that or proximately located data, can ...

SUM:

... volatility of magnetic disk, access times comparable to those of dynamic random-access memory (DRAM), and lower power consumption than either.

The current state of the art in flash memory management includes direct access to **read-only executable** programs or block-based access to read/write data.

Flash memory is regarded as a substitute for magnetic disk in many mass storage applications, particularly in laptop, palmtop, and ...

DRWDESC:

... shows a high-level flowchart illustrating the steps performed during use of an exemplary embodiment of the present invention.

FIG. 3 shows a high-level block diagram illustrating an exemplary virtual **memory map** employed by the present invention for the main and flash memories of FIG. 1.

FIG. 4 shows a functional block diagram illustrating the architecture of FIG. 1 with a memory management unit. ...

DETDESC:

... as fault trickling, exploits the fine-grained access capabilities of flash memory to gain back some of the lost performance. Although, the current state of the art in flash memory management includes direct access to **read-only executable** programs or block-based access to read/write data, until now the coordinated use of these two access techniques as in the fault trickling method have not been known.

FIG. 1 shows a ...

... fine-grain access to main memory 112 and flash memory 114. Direct access to flash memory 114 is made possible by the random access capabilities of flash memory and by support for **memory-mapped** input/output (I/O), which is provided by well known I/O **memory map** techniques.

According to the present invention, when data is requested, the MMU (shown in FIG. 4) determines whether the data is available from main memory 112 or if CPU 110 needs to access flash memory 114 to fetch the ...

... requests for data are honored from the new copy in main memory 112.

FIG. 3 is a functional block diagram which shows how data stored in the main memory 112 and flash **memory** 114 are **mapped** into a virtual memory space 310. The present invention directly maps data from flash memory to virtual memory while it performs the block transfer between flash memory 114 and main memory 112. It should be noted that the **memory map** is updated after each block transfer so the copy of data now located in main memory 112 is accessed once the block transfer is complete.

FIG. 4 is a functional block diagram similar to ...

... block transfers from flash memory 114 to main memory 112.

As indicated by the solid line drawn from address translation table (ATT) 430 to flash memory 114, on a first access, the **memory map** in ATT 430 maps the virtual address 440 supplied by the CPU 110 to the physical address 432 of flash memory 114.

It should be noted that, in the exemplary embodiment of the present invention, a " ...

... a block transfer of data from flash memory 114.

Thus, as indicated by the dotted line drawn from ATT 432 to main memory 112, on a second or

subsequent access of the same virtual address, the **memory map** in ATT 432 may be, for example, an associative **memory which maps** the virtual address located in the virtual address area 440 to the appropriate physical address, located in the physical address area 432, corresponding to main memory 112.

Although illustrated and described herein with reference to ...

... [*5] data by the CPU;

determining that the requested data is not stored in the main memory;

providing the CPU with direct single word access to the data from the flash memory device;

providing the accessed data to the CPU;

memory mapping virtual addresses of data not stored in the main memory device to physical address of the flash memory device;

concurrently with the direct single word access, commencing a block transfer of data, including the requested data, from the flash memory device to the main memory device; and

modifying, upon completion of the block transfer, the **memory map** such that the virtual addresses of data transferred to the main memory now correspond to physical addresses in the main memory rather than physical addresses in the flash memory.

[*6] 6. The method of claim 5, further comprising the ...

... [*6] concurrently with the directly accessing step,

commencing a block transfer of data, including the requested data, from the flash memory device to the main memory device.

[*7] 7. The method of claim 5, further comprising the step of

memory mapping virtual addresses of data not stored in the main memory device to physical address of the flash memory device.

[*8] 8. The method of claim 5, further comprising the step of

comparing the virtual address to an address ...

... [*10] unit;

concurrently with the direct single word access, commencing a block transfer of data, including the requested data, from the flash memory device to the main memory device; and

modifying, upon completion of the block transfer, the **memory map** such that the virtual addresses of data transferred to the main memory now correspond to physical addresses in the main memory rather

than physical addresses in the flash memory.

Source: Utility Patents
Search Terms: read only w/3 executable and memory w/2 map!
View: KWIC
Date/Time: Monday, March 29, 1999 - 9:40 AM EST

*Pat. No. 5440710, **

5,440,710

GET 1st DRAWING SHEET OF 8

Aug. 8, 1995

Emulation of segment bounds checking using paging with sub-page validity

INVENTOR: Richter, David E., San Jose, California
Cohen, Earl T., Fremont, California
Blomgren, James S., San Jose, California

CORE TERMS: segment, offset, virtual, sub-page, bit, memory, buffer, paging, byte, software...

SUM:

... bounds fault can be signalled by the translator.

Both segmentation and paging can be used for memory protection and management. Both perform a similar function in re-locating or **mapping** the user's **memory** references, and both can include accessibility attributes such as read-only, execute-only, dirty, and referenced. However, because segments may begin and end at any arbitrary address, not just at page boundaries, a separate ...

DETDESC:

... matching TLB entry and concatenated with the offset 52 to form the full 32-bit physical address 60.

Attributes stored in the TLB can include protection bits which can make a page **read-only, executable,** or writable for a particular user, and can also include reference bits which indicate if the data on the page has been modified and will need to be written back to a master storage area such as a disk ...

... segment to use in the instruction. The virtual address alone does not completely specify the memory location, since the same virtual address may exist in several different segments.

Segments 2 and 4 are **mapped** into the linear **memory** space 14 by a segmentation unit on the CPU.

Segment 2 has a base address 16 of 4000 bytes, which is 96 bytes below the beginning 18 of page 1 at 4096 bytes (4 ...

Source: Utility Patents
Search Terms: read only w/3 executable and memory w/2 map!
View: KWIC
Date/Time: Monday, March 29, 1999 - 9:41 AM EST